Frame synchronization algorithm of adaptive frame length system

Mingxue Bi *

Equipment engineering college, Shenyang Ligong University, Nanping Middle Str. 6, 110159 Shenyang, China

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Abstract

To solve the problem of identifying the alterable length frames, a specific frame synchronization algorithm is proposed in this paper. In the novel frame synchronization algorithm, the alterable length frames are demarcated by searching and checking the Attached Synchronization Marker bit by bit based on the altered frame format. Then the relevant performance parameters are analyzed and educed. The reference values for the rear protect time and the ahead protect time are given to ensure the probability of frame synchronization. Finally, the simulation results show that the novel frame synchronization algorithm can ensure the reliability of data transmitting and data processing for the adaptive frame length system.

Keywords: adaptive frame length, frame synchronization, z transform, reliability, attached synchronization marker

1 Introduction

In the wireless communication systems, the frame synchronization algorithm insures the reliability for backside data disposal by checking the frame synchronization marker and picking up the frame data. The performance of frame synchronization algorithm affects the whole communication performance for the wireless system firsthand. Up to the present, the frame synchronization technique and the relevant algorithms have been researched. And a mass of theory productions and application productions have been gained such as the selecting standard for synchronization header model, the searching arithmetic for synchronous header, design of appointed frame synchronization system, optimizing performance of frame synchronization, and so on [1]-[5].

With the development of wireless communications, the technique of adaptive frame length is produced to increase the system throughput in a certain extent [6]-[8]. But the variation characteristic of frame length adds the difficulty of frame synchronization enormously, and the existent algorithm of frame synchronization can not be usable to the adaptive frame length systems [9]. Aiming at the problem, the novel frame synchronization algorithm is produced to realize frame synchronization of the adaptive frame length system commendably. And reference values for the relevant frame synchronization parameters are presented to ensure the data reliability of transmission and disposal.

2 Design on frame synchronization algorithm

The design difficulty is that receiver needs to identify the variation of frame length (L_f) automatically, and find the Attached Synchronization Marker (ASM) to realize frame synchronization. So the Frame Length Marker (FLM) is defined between frame data and ASM just as Figure 1. The length of FLM is defined L_{FLM} bits. So it can marker $2^{L_{FLM}}$ kinds of L_f.

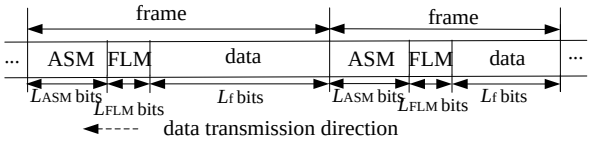

FIGURE 1 Serial bit sequence of adaptive frame length system.

In the data transmission process of the wireless communications, bit error in the ASM can be aroused by some factors such as environment noise, channel fading, and so on. That may induce the ASM with bit error to be leaked by receiver. It is a false leakage phenomenon. The random characteristics of bit sequence may induce the similar code piece of ASM appearing at the non-synchronization. If receiver mistakes it for ASM, the false alarm phenomenon is brought. Considering the effect of false leak and false alarm in searching and checking ASM, the error bit tolerance in ASM is defined to be N bits. The bit error rate of wireless channel is set as r, the false leak probability induced by the bit error of FLM is set as P_{FLM}, the false leakage probability induced by the bit error of ASM is set as P_{ASM}, and the false alarm probability is set as P_{FA}.

$$P_{ASM} = 1 - \sum_{j=0}^{N} \binom{L_{ASM}}{j} (1-r)^{L_{ASM}-j} r^j , \quad (1)$$

* Corresponding author E-mail: bmx418@163.com

$$P_{\mathrm{FLM}} = 1-(1-r)^{L_{\mathrm{FLM}}}, \tag{2}$$

$$P_{\mathrm{FA}} = \sum_{j=0}^{N}\binom{L_{\mathrm{ASM}}}{j}0.5^{L_{\mathrm{ASM}}}. \tag{3}$$

The design idea of the novel frame synchronization algorithm is searching and checking ASM bit by bit based on the altered frame format of Fig. 1. Namely, after searching ASM bit by bit successfully, the receiver checks next ASM bit by bit based on the frame length information of FLM. The frame synchronization states in the novel algorithm are introduced as follows.

- Frame synchronization searching state (Shorthand for S state) is the state of searching ASM bit by bit in the origination time of incepting data.
- Frame synchronization checking state (Shorthand for C state) is the state of reading frame length information in FLM and checking the next ASM bit by bit.
- Frame synchronization locking state (Shorthand for L state) is the state of locking the frame synchronization and dealing with frame data.
- Frame synchronization holding state (Shorthand for H state) is the state of reading ASM, checking the next ASM bit by bit and taking count of holding synchronization.

The states transfer process of the novel frame synchronization algorithm is shown as Figure 2

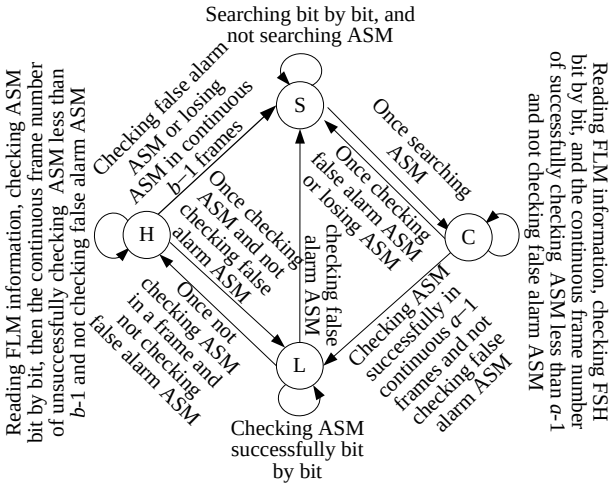

FIGURE 2 States transfer process of the novel algorithm.

Hereinto, a is the rear protect time, and b is the ahead protect time. In order to reduce the false synchronization probability caused by the ASM false alarm, only when checking ASM successfully in continuous a frames, system locks the frame synchronization. In order to reduce the false synchronization loss probability caused by the ASM false leakage or the FLM error, only when checking ASM unsuccessfully in continuous b frames, system determines the frame synchronization loss.

2.1 FRAME SYNCHRONIZATION SEARCHING AND CHECKING PROCESS

The frame synchronization searching and checking process of the novel algorithm is shown as Figure 3.

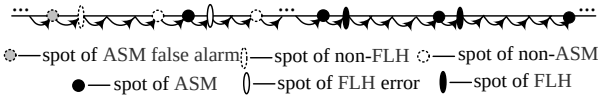

FIGURE 3 Frame synchronization searching and checking process.

Beginning to receive the data or losing the frame synchronization, system enters the S state to search ASM bit by bit. Once searching ASM, system stops searching and enters the C state. In the C state, system searches the ASM bit by bit continuously. Once the next ASM is found, the system extracts the information of frame length (L_{f}) depending on the adjacent two ASM. If L_{f} meets the specified frame length, system judges the ASM is true and checks the next one bit by bit continuously. On the other hand, system judges the previous ASM is the false alarm ASM and returns the C state again to check the ASM bit by bit. If not checking the ASM within the specified range of frame length, system judges the previous ASM is the false alarm ASM and returns the S state. If ASM is checked successfully in continuous $a-1$ frames of the C state, system will enter the L state. The time of searching and checking process is defined as the time of system entering lock T_{EL}.

2.2 FRAME SYNCHRONIZATION LOCK AND KEEP PROCESS

The frame synchronization locking and holding process of the novel arithmetic is shown as Figure 4.

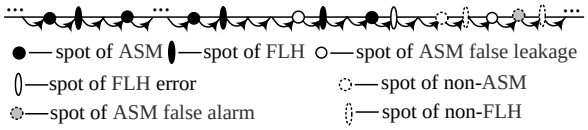

FIGURE 4 Frame synchronization locking and holding process.

Once entering L state, system starts to deal with frame data from the previous a frame, but still reads the frame length information of FLM and checks ASM bit by bit. The frame synchronization locking and holding process can be divided into two cases as follows.

- Considering possible error in ASM and FLM, system does not return S state immediately but enters H state as losing ASM in one frame. In H state, reading L_{f} information in FLM, system checks ASM in the start of next frame. If checking ASM unsuccessfully in continuous $b-1$ frames in H state, system determines the frame synchronization loss, enters S state, and stops

dealing with frame data. Otherwise, system returns L state.

- Once checking the ASM in the no specified frame length and no the FLM specified position, system enters the S state immediately.

Only considering bit error in system, the holding process can be separated into the holding process I (H_I for short) caused by the FLM error and the ASM false leakage at the same time and the holding process II (H_{II} for short) caused by ASM false leakage only. The processes of H_I and H_{II} are shown as Figure 5 (a) and Figure 5 (b) respectively.

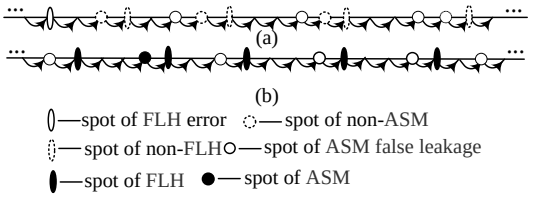

FIGURE 5 Frame synchronization holding process.

As FLM error and ASM false leakage at the same time in H_I, the real ASM will not exist in the start of next frame specified by FLM. So the ASM loss caused by FLM error and ASM false leakage at the same time is true. If not checking out ASM for false alarm in the starts of continuous $b-1$ frames, system enters S state. Obviously, during the H_I process caused by FLM error, the frame data dealt with are false. So the time through H_I process is defined as the time of system releasing from error lock T_{CL}. T_{CL} and T_{EL} are defined as the continuance time of losing frame synchronization T_L. The ASM loss only caused by ASM false leakage is false in H_{II}. But if ASMs in the starts of continuous $b-1$ frames are not checked out for false leakage, system enters S state. Obviously, during the H_{II} process only caused by ASM false leakage, the frame data dealt with are correct. So the time through H_{II} process and locking process is defined as the continuance time of frame synchronization T_H.

3 Performance analysis of novel frame synchronization algorithm

Without regard to the influence of system code sliding, the transfer probabilities between four states of the novel frame synchronization algorithm are constant. So the frame synchronization process is a discrete Markov process. The z transform method is used for the performance analysis of novel frame synchronization algorithm.

3.1 PERFORMANCE ANALYSIS OF ENTERING LOCK

Assuming system checking ASM from any bit of any frame, the average probability for true ASM being searched successfully but FLM not being read in the frame (P_{T1} for short) can be given.

$$P_{T1}=\frac{1-P_{ASM}}{L_f}\sum_{k=1}^{L_f}(1-P_{FA})^{k-1}=\frac{(1-P_{ASM})[1-(1-P_{FA})^{L_f}]}{L_f P_{FA}}. \tag{4}$$

The average probability of frame synchronization entering locking P_{EL} can be given:

$$P_{EL}=P_{T1}(1-P_{ASM})^{a-1}(1-P_{FA})^{(a-1)N_f}$$

$$=\frac{(1-P_{ASM})^a(1-P_{FA})^{(a-1)N_f}[1-(1-P_{FA})^{L_f}]}{L_f P_{FA}}. \tag{5}$$

The adaptive frame length system generally is used in slow fading channel. So under the great frame quantity, the average frame length is assumed as L bit. Letting $P=(1-P_{ASM})(1-P_{FA})^L$, the states transfer process of frame synchronization searching and checking is shown as Figure 6.

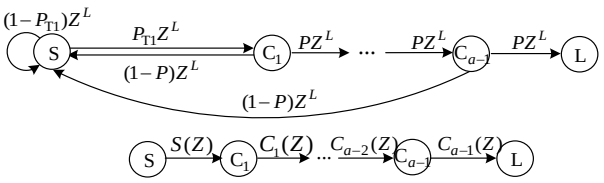

FIGURE 6 States transfer of frame synchronization searching and checking.

The z transformation for each state transfer probability is given respectively.

$$S(Z)=\sum_{m=0}^{\infty}\left[(1-P_{T1})Z^L\right]^m P_{T1}Z^L=\frac{P_{T1}Z^L}{1-(1-P_{T1})Z^L}, \tag{6}$$

$$C_i(Z)=\frac{PZ^L}{1-S(Z)\prod_{j=0}^{i-1}C_j(Z)(1-P)Z^L}. \tag{7}$$

Hereinto, $i=1, 2, \ldots, a-1$, $C_0(Z)=1$. T_{EL} normalized to L can be obtained.

$$T_{EL}=\frac{1}{L}\left[d\left(S(Z)\prod_{i=1}^{a-1}C_i(Z)\right)\Big/dZ\right]\Big|_{Z=1}$$

$$=\frac{1+P_{T1}-P-P_{T1}P^{a-1}}{P_{T1}(1-P)P^{a-1}}. \tag{8}$$

3.2 PERFORMANCE ANALYSIS OF LOSING FRAME SYNCHRONIZATION

As FLM error and ASM false leakage at the same time, system enters the H_I process shown as Figure 7,

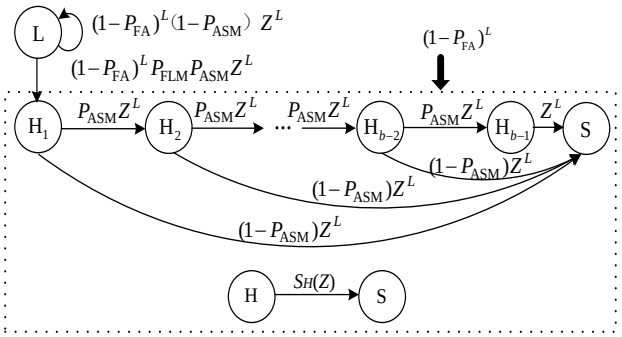

FIGURE 7 States transfer of H_I process.

where

$$S_H(Z)=(1-P_{\mathrm{ASM}})Z^L\sum_{m=0}^{b-3}(P_{\mathrm{ASM}}Z^L)^m+(P_{\mathrm{ASM}}Z^L)^{b-2}Z^L$$

$$=\frac{P_{\mathrm{ASM}}^{b-1}Z^{L(b-1)}-P_{\mathrm{ASM}}^{b-1}Z^{Lb}-P_{\mathrm{ASM}}Z^L+Z^L}{1-P_{\mathrm{ASM}}Z^L}. \tag{9}$$

The normalized time from the H_1 state to the S state can be obtained:

$$T_{\mathrm{LC1}}=\frac{1}{L}\frac{dS_H(Z)}{dZ}\bigg|_{Z=1}=\frac{1-P_{\mathrm{ASM}}^{b-1}}{1-P_{\mathrm{ASM}}}. \tag{10}$$

Then, as FLM error and ASM false leakage at the same time, the time of confirming frame synchronization loss T_{LC} can be given:

$$T_{\mathrm{LC}}=\frac{1}{L}\frac{d[(1-P_{\mathrm{FA}})^L P_{\mathrm{FLM}}P_{\mathrm{ASM}}Z^L(1-P_{\mathrm{FA}})^{(b-1)L}S_H(Z)]}{dZ}\bigg|_{Z=1}$$

$$=\frac{(1-P_{\mathrm{FA}})^{bL}(2-P_{\mathrm{ASM}}^{b-1}-P_{\mathrm{ASM}})P_{\mathrm{FLM}}P_{\mathrm{ASM}}}{1-P_{\mathrm{ASM}}}. \tag{11}$$

The normalized time of frame synchronization loss T_{L} can be obtained as

$$T_{\mathrm{L}}=T_{\mathrm{EL}}+T_{\mathrm{LC}}. \tag{12}$$

The average probability of frame synchronization loss P_{L} can be obtained as:

$$P_{\mathrm{L}}=P_{\mathrm{FA}}+(1-P_{\mathrm{FA}})^{bL}[P_{\mathrm{FLM}}P_{\mathrm{ASM}}(1-P_{\mathrm{ASM}})+P_{\mathrm{ASM}}^b]. \tag{13}$$

3.3 PERFORMANCE ANALYSIS OF CONTINUANCE SYNCHRONIZATION

The state transfer of frame synchronization locking and H_{II} process is shown as Figure 8,

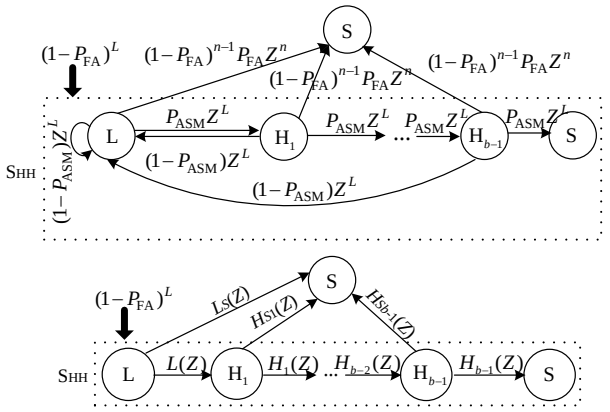

FIGURE 8 State transfer of frame synchronization locking and H_{II} process.

where

$$L(Z)=\frac{P_{\mathrm{ASM}}Z^L}{1-(1-P_{\mathrm{ASM}})Z^L}, \tag{14}$$

$$H_q(Z)=\frac{P_{\mathrm{ASM}}Z^L}{1-L(Z)\prod_{j=0}^{q-1}H_j(Z)(1-P_{\mathrm{ASM}})Z^L}. \tag{15}$$

Hereinto, q=1,2,…,b−1, $H_0(Z)$=1. The normalized time T_{H11} from L to S state in S_{HH} process is given:

$$T_{\mathrm{H11}}=\frac{1-P_{\mathrm{ASM}}^b}{(1-P_{\mathrm{ASM}})P_{\mathrm{ASM}}^b}. \tag{16}$$

Only when ASM is false leakage, the normalized time T_{H1} is given:

$$T_{\mathrm{H1}}=(1-P_{\mathrm{FA}})^{(b+l)L}T_{\mathrm{H11}}=\frac{(1-P_{\mathrm{FA}})^{(b+l)L}(1-P_{\mathrm{ASM}}^b)}{(1-P_{\mathrm{ASM}})P_{\mathrm{ASM}}^b}, \tag{17}$$

$$l=\frac{1}{L}\left[d\sum_{m=0}^{\infty}\left[(1-P_{\mathrm{FA}})^L(1-P_{\mathrm{ASM}})Z^L\right]^m/dZ\right]\bigg|_{Z=1}$$

$$=\frac{(1-P_{\mathrm{FA}})^L(1-P_{\mathrm{ASM}})}{[1-(1-P_{\mathrm{FA}})^L(1-P_{\mathrm{ASM}})]^2}. \tag{18}$$

If ASM is false alarm, system enters the S state. $(1-P_{\mathrm{FA}})^{n-1}P_{\mathrm{FA}}$ refers to the probability of the top n−1 bits being not false alarm and the n bit being false alarm in one frame.

$$L_S(Z)=\frac{(1-P_{FA})^{Ll+n-1}P_{FA}Z^nL(Z)}{P_{ASM}Z^L}$$

$$=\frac{(1-P_{FA})^{Ll+n-1}P_{FA}}{P_{ASM}}L(Z)Z^{n-L}, \quad (19)$$

$$H_{Sq}(Z)=\frac{(1-P_{FA})^{L(l+q)+n-1}P_{FA}}{P_{ASM}}H_q(Z)Z^{n-L}. \quad (20)$$

The normalized time from S_{HH} to S state leaded by false alarm ASM can be obtained:

$$T_{H2}=\frac{1}{L}\frac{dL_S(Z)}{dZ}\bigg|_{Z=1}+\frac{1}{L}\frac{d[L(Z)H_{S1}(Z)]}{dZ}\bigg|_{Z=1}$$

$$+...+\frac{1}{L}d[L(Z)\prod_{q=1}^{b-2}H_q(Z)H_{Sb-1}(Z)]/dZ\bigg|_{Z=1}. \quad (21)$$

Let $n=L/2$ and $T_{H2}(0)=0$, then under the different b, $T_{H2}(b)$ can be gotten:

$$T_{H2}(b)=\frac{P_{FA}(1-P_{FA})^{L(l+b+1/2)-1}}{P_{ASM}^{b+1}}(\sum_{i=0}^{b-1}P_{ASM}^i-\frac{P_{ASM}^b}{2})+\sum_{k=0}^{b-1}T_{H2}(k), \quad (22)$$

Then, the normalized continuance time of frame synchronization T_H is obtained.

$$T_H=T_{H1}+T_{H2}. \quad (23)$$

4 Performance simulation and parameters design of novel algorithm

Simulation map of frame synchronization process is shown as Figure 9. The bit data generator produces 10^8 bit data each time. $L_f \in$ {100 byte, 500 byte, 1000 byte, 2000 byte} and each L_f is appeared by equal probability. L=900 byte, N=2 bit, L_{FLM}=2 bit and ASM$\in${00, 01, 10, 11} represents each L_f separately. ASM is selected as 00011010110011111111110000011101 [10] for ensuring the false alarm probability to be low enough ($P_{FA}\approx10^{-7}$). Obviously, L_{ASM}=32 bit.

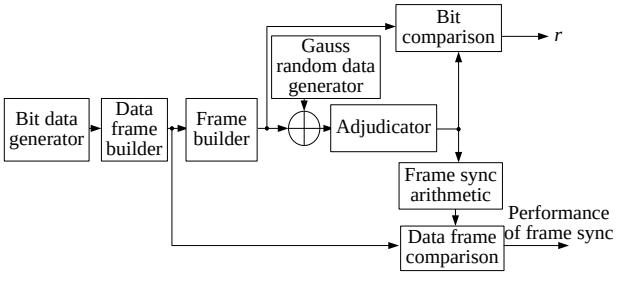

FIGURE 9 Simulation map of frame synchronization process.

4.1 PARAMETERS ANALYSIS OF ENTERING LOCK

The computation results and simulation results about the probability of system entering lock P_{EL} and the time of system entering lock T_{EL} are shown as Figure 10 and Figure 11 respectively.

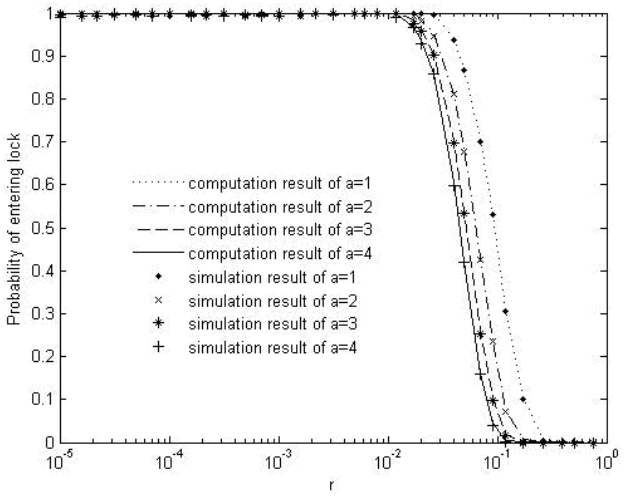

FIGURE 10 Probability of entering lock P_{EL}.

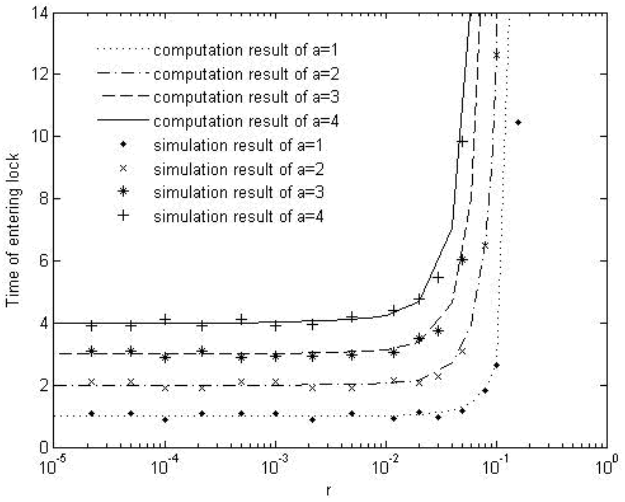

FIGURE 11 Time of entering lock T_{EL}.

Combined with Figure 10 and Figure 11, the phenomena of P_{EL} overall decreasing with the increase of r, and the phenomena of T_{EL} increasing with the increase of r can be seen obviously. When $r\geq10^{-2}$, with the increase of r, P_{EL} decreased rapidly until to zero, but T_{EL} increases rapidly for very large values. a is greater, P_{EL} depresses and T_{EL} increases faster. Because, in the process of searching ASM bit by bit and checking ASM frame by frame, the increase of r and a leads ASM and FLM to be leaked frequently. So P_{EL} is reduced and T_{EL} is prolonged. When the channel condition is good (namely r is smaller), P_{EL}=1 and T_{EL} is only related to the value of a (namely $T_{EL}=a$). Therefore, for increasing P_{EL}

and decreasing T_{EL}, the smaller value of a should be taken. But if selecting the very small value for a, system will enter frame synchronization easily. Then the data processing reliability can not be ensured. So a=2 can be chosen in the actual system.

4.2 PARAMETERS ANALYSIS OF LOSING FRAME SYNCHRONIZATION

The computation results and simulation results about the time of system confirming frame synchronization loss T_{LC1} and T_{LC} are shown as Figure 12 and Figure 13.

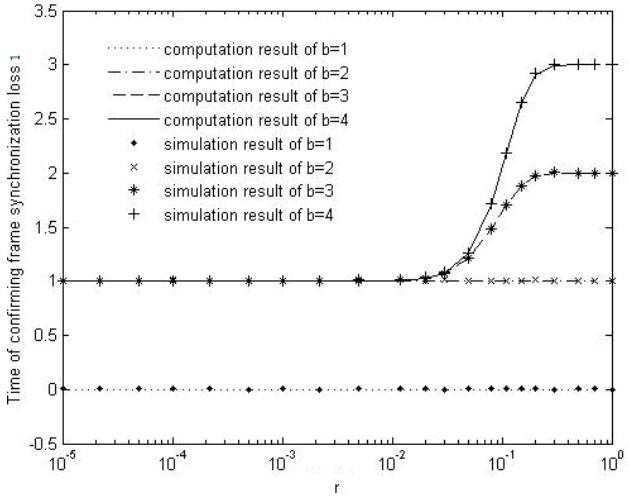

FIGURE 12 Time of confirming frame synchronization loss T_{LC1}.

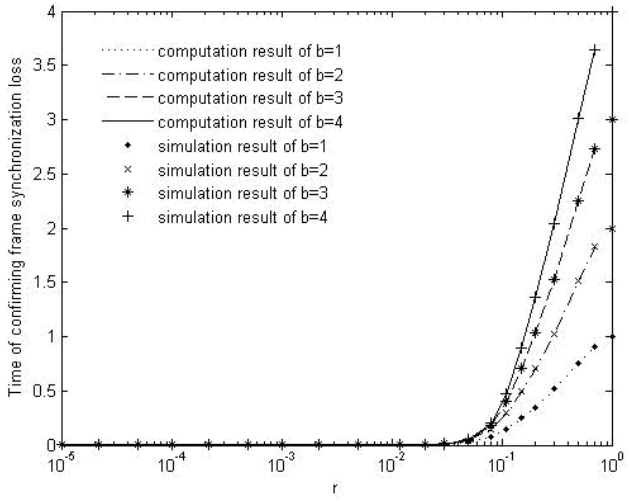

FIGURE 13 Time of confirming frame synchronization loss T_{LC}.

Figure 12 shows that, when the ahead protect time b=1, the time of confirming frame synchronization loss T_{LC1}=0. when b=2, T_{LC1}=1. The reason is that when b=1, there is not the H_I process. So T_{LC1}=0. When b=2, system only needs check one frame in the holding frame synchronization process. So no matter what value of the bit error rate r, T_{LC1}=1. As $b\geq3$, if r is low, T_{LC1}=1; but if $r\geq10^{-2}$, T_{LC1} increases along with enhancing of r until to close the value of $b-1$. The reason is that when the channel condition is good, the value of P_{ASM} will be small. So system will check out the ASM easily in the next frame. But this ASM will be thought as a false alarm ASM. system will enter into the S status, and T_{LC1}=1. When the channel condition is bad, the value of P_{ASM} will be large. System will miss the ASM frequently and T_{LC1} will be extended. When the channel condition is worst, the ASMs of continuous $b-1$ frames will be missed and $T_{LC1}=b-1$.

Figure 13 shows that, when $r\leq10^{-2}$, $T_{LC}\approx0$. When $r>10^{-2}$, T_{LC} increases along with enhancing of r until to close the value of b. The reason is that when the channel condition is good, the value of $(1-P_{FA})P_{ASM}P_{FLM}$ is very small. So the probability of system enters the H_I process is very low. At this time, $T_{LC}\approx0$. But when the channel condition becomes bad, increase in the values of P_{ASM} and P_{FLM} improve the probability of system enters the H_I process gradually. As the channel condition is worst, the all ASMs in the continuous b frames will be missed. At this time, $T_{LC}=b$.

As a=2, the computation results and simulation results about the probability of system losing frame synchronization P_L and the time of system losing frame synchronization T_L are shown as Fig. 14 and 15.

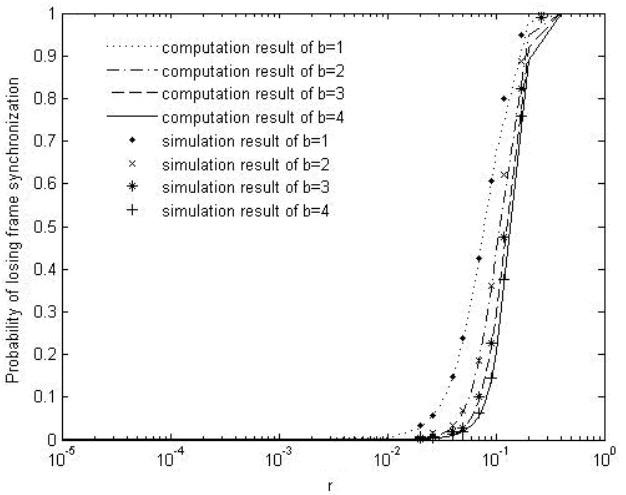

FIGURE 14 Probability of losing frame synchronization P_L.

Figure 14 shows that, when $r\leq10^{-2}$, $P_L\approx0$ no matter what value of b. when $r>10^{-2}$, P_L increases along with enhancing of r until to close the maximum 1. And b is smaller, P_L increases more rapidly. The reason is that when the channel condition is good, P_{FLM} and P_{ASM} are very small. Then system can keep in the L state or the H state. P_L is very low. As the channel condition becomes bad, P_{FLM} and P_{ASM} increase gradually. Here if b is smaller, the probability of system keeping in the L state and H state is lower, so P_L is higher. Therefore, in order to reduce the P_L, the larger value of b should be taken.

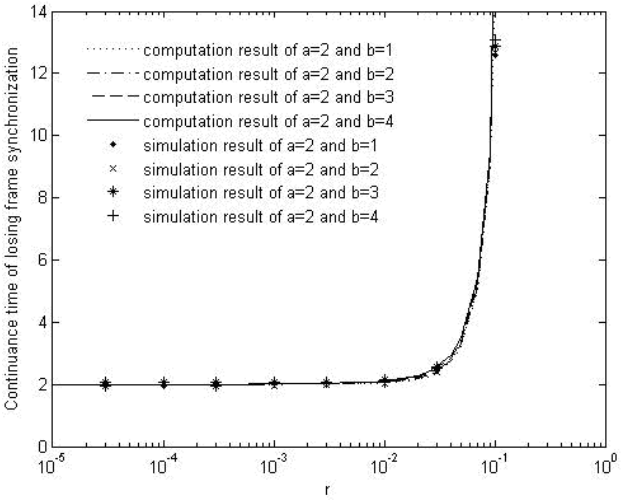

FIGURE 15 Continuance time of losing frame synchronization T_L.

Figure 15 shows that, T_{EL} increases with the enhancing of r. When $r \geq 10^{-2}$, with the enhancing of r, T_{EL} increases rapidly for very large values. Combined with Fig. 11, Fig. 13 and Fig.15, it can be seen that $T_L \approx T_{EL}$ for the lower T_{LC}. Namely, when the channel condition is good, $T_L=a=2$, and when the channel condition is very bad, T_L will tend to the infinity value.

4.3 PARAMETERS ANALYSIS OF CONTINUANCE FRAME SYNCHRONIZATION

The computation results and simulation results about continuance time of system holding frame synchronization T_H are shown as Figure 16.

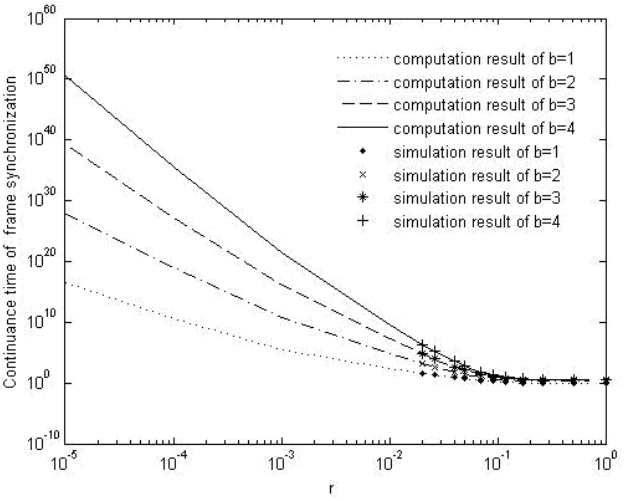

FIGURE 16 Continuance time of frame synchronization T_H.

Obviously, when the channel condition is good, P_{FLM} and P_{ASM} are very low and $P_{ASM} << P_{FLM}$. Then system will keep in the H_{II} process. And b is larger, the time in H_{II} process is longer, and T_H is larger. When the channel condition is bad, P_{FLM} and P_{ASM} are large. ASM will be lost frequently. Then T_H is smaller. Therefore, for improving T_H, the larger value of b should be taken.

However, L_f in adaptive frame length system is not the fixed value. Once losing the ASM of a frame for the error FLM, system will lose all the data contained in the frame. Therefore, for increasing the reliability of data processed, the value of b should not be too large. In conclusion, b=3 can be choose for the novel algorithm.

4.4 PERFORMANCE COMPARISON ANALYSIS OF DIFFERENT FRAME SYNCHRONIZATION ALGORITHMS

The computation results about probability of frame synchronization entering lock, probability of frame synchronization loss, continuance time of frame synchronization, and continuance time of frame synchronization loss for the novel algorithm in this paper and the original algorithm in [11] are shown from Figure 17 to Figure 20.

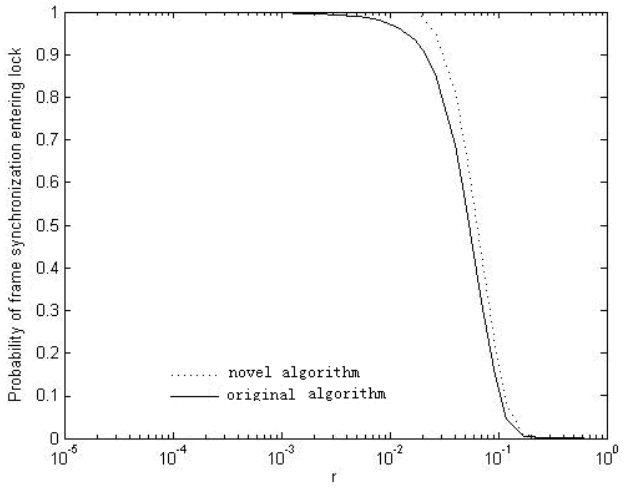

FIGURE 17 Probability of frame synchronization entering lock.

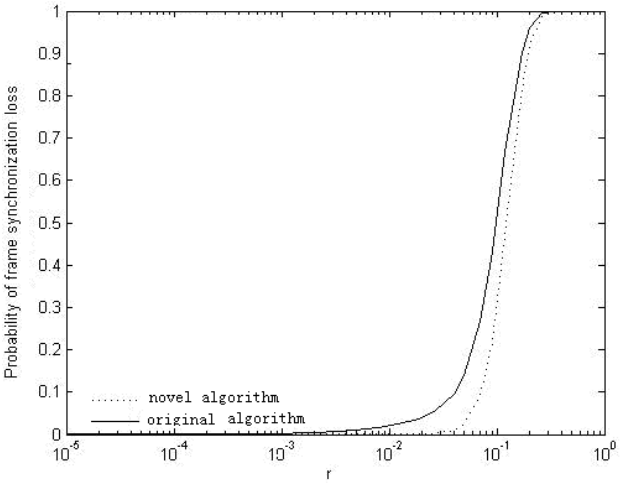

FIGURE 18 Probability of frame synchronization loss.

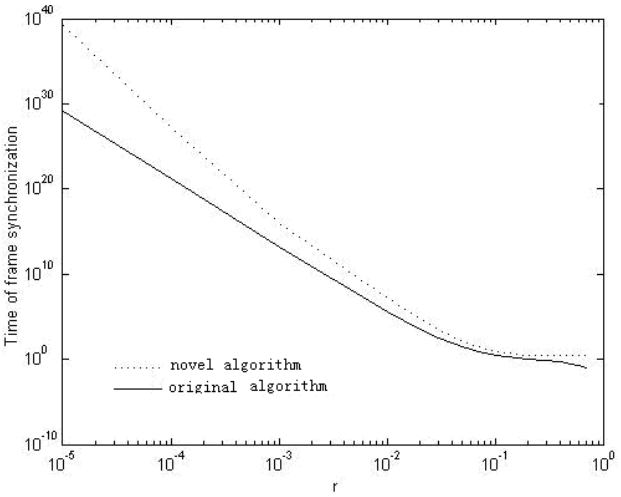

FIGURE 19 Continuance time of frame synchronization.

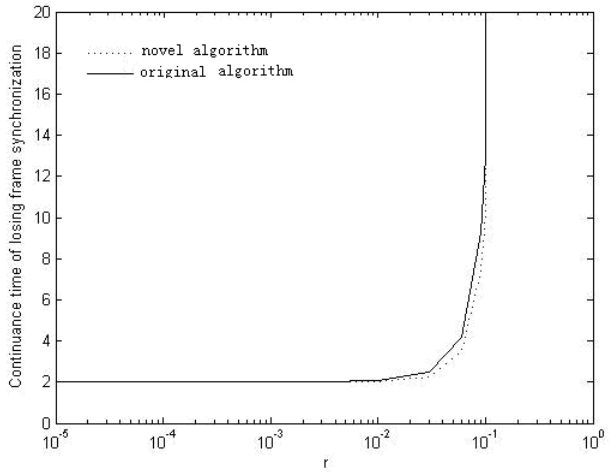

FIGURE 20 Continuance time of frame synchronization loss.

According to the overall link state ($10^{-5} \le r \le 10^{0}$), the probability of frame synchronization entering lock in novel algorithm improves by 21.04% compared to the original arithmetic in Figure 17. The probability of frame synchronization loss in novel arithmetic reduced by 6.15% compared to the original arithmetic in Figure 18. The continuance time of frame synchronization in novel algorithm improves by 10 times compared to the original arithmetic in Figure 19. Only the continuance time of frame synchronization in novel algorithm loss is similar to the original arithmetic in Figure 20.

The results of Figure 17, Figure 18, and Figure 19 show that the novel algorithm can enter and hold the frame synchronization more easily. Obviously, the novel algorithm performance is superior of the original algorithm.

5 Conclusions

In view of the problem that the traditional frame synchronization algorithms can not identify the variation length frame, a novel algorithm is presented in this paper. First, the traditional frame format is improved by setting the FLM. The FLM with the length of L_{FLM} bits can market $2^{L_{FLM}}$ kinds of L_f. According to the information of L_f in FLM, system can check ASM bit by bit to lock or hold frame synchronization after searching out ASM bit by bit. Then, the performance parameters of the novel algorithm are educed, such as the probability of system entering frame synchronization lock, the probability of system losing frame synchronization, the continuance time of system holding frame synchronization, the continuance time of system losing frame synchronization, and so on. The significance of solving the problem is to ensuring the reliability of data transmitting and processing for the adaptive frame length system. And the reference values for the rear protect time *a* and the ahead protect time *b* are given by simulating and analyzing. Based on those, the novel frame synchronization arithmetic can resolve the frame synchronization limit of fixed frame length and ensure the probability of frame synchronization and the reliability of data transmitting and processing in variable frame length system. Finally, compared with the original algorithm, the novel frame synchronization arithmetic can enter and hold the frame synchronization more easily.

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Authors

Bi Mingxue , 1980-04-18, Weihai City Shandong Province

Current position, grades: teacher, graded the Doctor degree from Nanjing University of Science and Technology
University studies: communications and navigation technology
Scientific interest: the Adaptive Transmission technology
Publications: Research on High QoS Two-Class Multiplexing Algorithm(Beijing: ACTA ARMAMENTARII, 2013); Research on Transmission Arithmetic of AOS Adaptive Frame Length System(Beijing: Acta Aeronautica et Astronautica Sinica, 2012)
Experience: Wireless communication technology